

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A data transfer system comprising:
2 a plurality of bus devices, at least one bus device being a
3 bus data supplying device capable of supplying data, at least one
4 bus device being a bus data receiving device capable of receiving
5 data and at least one bus device being a bus master device capable
6 of requesting and controlling data transfer;
7 a data bus connected to each of said plurality of bus devices
8 and capable of transferring data from a bus data supplying device
9 to a bus data receiving device under control of a bus master
10 device;
11 a direct memory access unit connected to said data bus as a
12 bus master device, said direct memory access unit including
13 a source word size register storing a source word size,
14 and
15 a target word size register storing a target word size,
16 a source start address register storing a source start
17 address,
18 a source increment size register storing a source
19 increment size,
20 a target start address register storing a target start
21 address, and
22 a target increment size register storing a target
23 increment size,
24 said direct memory access unit capable of transferring data from a
25 first bus data supplying device to a first bus data ~~recalling~~
26 receiving device via said first bus by recalling data from a first
27 bus data supplying device beginning at said source start address
28 and thereafter at successive addresses differing by said source

29 increment size in a data size corresponding to said source word
By 30 data size and supplying said recalled data to a first bus data
31 receiving device beginning at said target start address and
32 thereafter at successive addresses differing by said target
33 increment size in a data size corresponding to said target word
34 size.

1 2. (Original) The data transfer system of claim 1, wherein:
2 said direct memory access unit further includes
3 a read data register loaded with data from said bus data
4 supplying device via said data bus in said source word size,
5 a write data register supplying data to said bus data
6 receiving device via said data bus in said target word size,
7 and
8 a word formatter connected to transfer data from said
9 read data register to said write data register thereby
10 aligning data in said target word size in said write data
11 register.

1 3. (Original) The data transfer system of claim 2, further
2 comprising:
3 at least one first bus device being a first bus
4 supplying/receiving device capable of both supplying data to said
5 first bus and receiving data from said first bus.

1 4. (Original) The data transfer system of claim 3, wherein:
2 at least one first bus supplying/receiving device consists of
3 a central processing unit which is further capable of controlling
4 data transfer.

34

1 5. (Original) The data transfer system of claim 3, wherein:
2 at least one first bus supplying/receiving device consists of
3 a direct memory access unit which is further capable of controlling
4 data transfer.

1 6. (Original) The data transfer system of claim 3, wherein:
2 at least one first bus supplying/receiving device consists of
3 a memory which is not capable of controlling data transfer.

1 7. (Original) The data transfer system of claim 3, wherein:
2 at least one first bus supplying/receiving device consists of
3 a central processing unit which is further capable of controlling
4 data transfer, said central processing unit connected to said
5 direct memory access unit for loading data into said source data
6 size register and into said target data size register.

8. (Canceled)

1 9. (Currently Amended) The data transfer system of claim ~~8~~ 1,
2 wherein:
3 at least one first bus supplying/receiving device consists of
4 a central processing unit which is further capable of controlling
5 data transfer, said central processing unit connected to said
6 direct memory access unit for loading data into said source start
7 address register, said source increment size register storing, said
8 target start address register and said target increment size
9 register.

1 10. (Currently Amended) The data transfer system of claim ~~3~~
2 1, further comprising:
3 a bus arbiter connected to each of said at least one bus
4 master device, said direct memory access unit and said first bus,

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5 said bus arbiter granting control of data transfer on said data bus
6 to one and only one bus master device; and
7 said direct memory access unit further includes
8 a counter value register storing a number of data words
9 to be transferred by said direct memory access unit,
10 a block size register storing a block size to be
11 transmitted without interruption,
12 said direct memory access unit requesting bus control from said bus
13 arbiter and upon grant of control of data transmission on said data
14 bus, said direct memory access unit thereafter
15 transferring data in an amount equal to the lesser of
16 said number of data words to be transferred and said block
17 size to be transmitted without interruption, thereafter
18 ending data transfer if data transferred equals said
19 number of data words to be transmitted, and
20 suspending data transfer, releasing control of data
21 transfer on said data bus and re-requesting bus control from
22 said bus arbiter.

1 11. (Original) The data transfer system of claim 10, wherein:
2 at least one first bus supplying/receiving device consists of
3 a central processing unit which is further capable of controlling
4 data transfer, said central processing unit connected to said
5 direct memory access unit for loading data into said counter value
6 register and said block size register.

1 12. (Original) The data transfer system of claim 1, wherein
2 said plurality of bus devices consist of first bus devices and said
3 data bus consists of a first data bus, said data transfer system
4 further comprising:
5 a plurality of second bus devices, at least one second bus
6 device being a second bus data supplying device capable of

7 supplying data, at least one second bus device being a second bus
8 data receiving device capable of receiving data and at least one
9 second bus device being a second bus master device capable of
10 requesting and controlling data transfer, each second bus device
11 having a predetermined data size;
12 a second data bus having said predetermined data size
13 connected to each of said plurality of second bus devices and
14 capable of transferring data from a second bus data supplying
15 device to a second bus data receiving device under control of a
16 second bus master device;
17 a bus bridge connected to said first data bus and said second
18 data bus, said bus bridge capable of transferring data between said
19 first bus devices and said second bus devices; and
20 wherein said direct memory access unit stores said
21 predetermined data size in said source word size register for data
22 transfer from a second bus device to a first bus device via said
23 bus bridge and stores said predetermined data size in said target
24 word size register for data transfer from a first bus device to a
25 second bus device via said bus bridge.

In the Drawings

Figure 2: Add legend "(PRIOR ART)".